THE PLASMA CONNECTION

IEEE NPSS NUCLEAR & PLASMA SCIENCES SOCIETY

FROM THE IEEE NUCLEAR & PLASMA SCIENCES SOCIETY

JUNE 2023

Plasma for Microelectronics

MIRKO VUKOVIC

TEL TECHNOLOGY CENTER, AMERICA, LLC

Introduction

Most readers of this column are exposed to the benefits of microelectronics daily. Examples include connectivity, entertainment, productivity, automotive and health.

The pervasiveness of microelectronics is driven by their performance and affordability. The economic force that enabled the democratization of microelectronics is referred to as Moore's law. It states that the number of transistors on a silicon wafer doubles every 18-36 months, which leads to a decrease in cost/transistor while the performance (speed, power consumption) is improved (see Figure 1). This has led to miniaturization of computers, phones, and other devices while at the same time increasing their functionality.

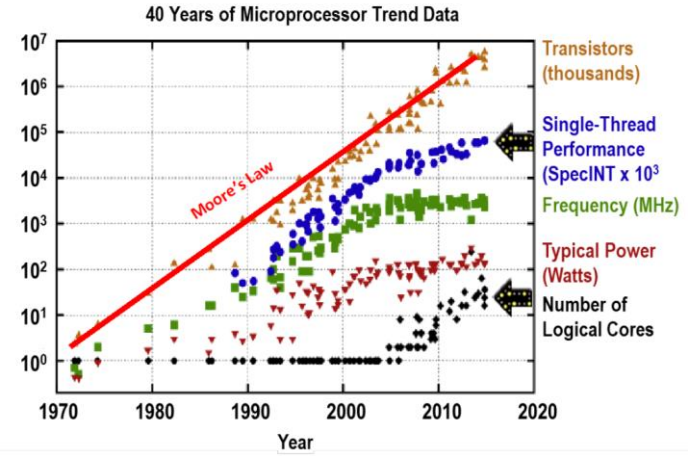


Figure 1 Growth in the number of transistors/microprocessor over the past 5 decades (IRDS Executive Summary, 2022). While the number of transistors follows Moore's law, power has leveled off in the early 2000's to prevent damage from very intense heat dissipation. This forced the increase in clock frequency to level off. In turn, single improvements thread performance gains have slowed down. Additional performance gains are obtained by including multiple cores in the chips. (© 2022 IEEE)

Plasmas (ionized gases) are one of the key technologies used in microelectronic fabrication that facilitate Moore's law. Plasma processing happens at pressures of less than 1/10,000 of atmospheric pressure (corresponding to a height of about 90 km above the earth surface) and under exceptionally clean and controlled conditions.

This technology has been used since the 1970's in the semiconductor industry (IRDS More Moore, 2022). The basic technological and process components were identified and in place by the mid 1990's, so that an RF or process engineer from that era would easily understand most components of today's equipment. However, the equipment and process from that era would not be capable of producing even one functioning CPU chip for today's smartphone. To understand what drives the change in microelectronic manufacturing technology (and this include plasma-based technologies) consider the changes from the 1970's, when plasmas-based process technology was introduced, to early 2020's:

- The number of transistors on a chip has gone from 10's of thousands to 100's of billions.
    - The number of distinct components (such as interconnecting wires) is reaching into a trillion.
- The dimensions of some of circuit components has decreased from 3µ to 30 nm.
    - Some critical dimensions measure in single nm.
- The number of materials used has gone from ~10 to >30.
- The wafer size has increased from 4 in to 12 in.
- The number of steps in making a chip has gone from ~100 to ~1500.

Modern chip architectures and their fabrication

From left to right on Figure 2 are transistors such as in logic chips (CPU), 3D-NAND memory arrays that are used in solid state drives, and DRAM memory. The horizontal dimensions are of the order of 100 nm or less. The vertical dimensions range from 10's of nanometer to microns. The individual components of these structures are either semiconductors (for operation of transistors), conductors (for signal, power, and timing propagation) or dielectrics (for mechanical strength and electrical insulation).

All these devices are fabricated layer by layer through a repetition of three basic processing steps:

1. Deposition of a thin layer of material (metal or dielectric).
2. Deposition of a photo-sensitive layer on which a pattern is optically transferred.
3. Transfer of the pattern from the photo-sensitive layer to the layers underneath.

For the industry to remain profitable and to be able to invest in future generations of product and equipment, the manufacturing yield has to approach 90%. That means that 90% of the chips on a wafer need to have all trillion components satisfy stringent quality requirements over the course of 1000+ process steps.

While this task looks formidable or even impossible, it is made possible by decades of long, steady, mostly incremental improvement in process and equipment, gain in knowledge and experience of large number of technicians, engineers, scientists & researchers from many disciplines.

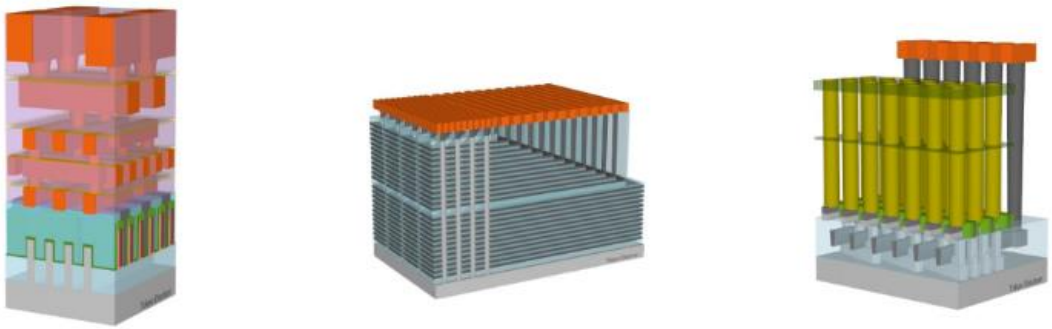


Figure 2 Examples of modern architectures: A) A Logic cell with transistors and their first 4 levels of interconnecting wires. B) A Cross-section of a 3D-NAND memory cell in which upwards of 20 transistors are stacked vertically around the vertical 4 visible vertical channels. C) A cross-section of DRAM memory with the transistors at the bottom, and tall slender capacitors above them store the electrons for the memory bit. (Source: TEL)

Plasma generation

Plasma as a tool was introduced in the 1970's to strip organic layers from wafers. From that early application plasma processing propagated into pattern transfer, as it was the only way to transfer patterns vertically into the Silicon wafer and other layers. The role of plasma then expanded into deposition of both metals and dielectrics.

The processing plasma is created by application of an electric field to a gas mixture to create a gas discharge similar to a spark in dry air or to lightening. Unlike these examples, plasmas used in the microelectronic industry are created under very low pressure, which gives them unique properties that are used to their advantage in the computer chip fabrication. Figure 3 shows an example of such plasma.

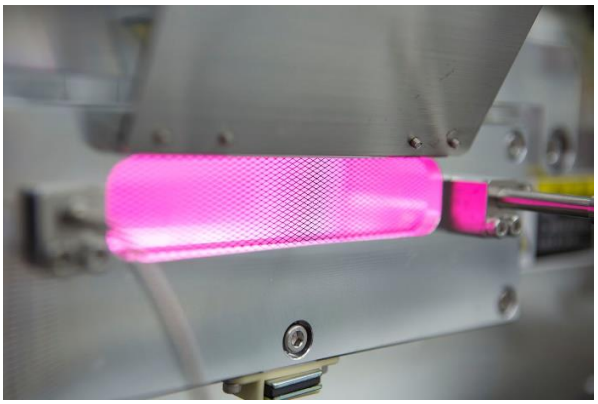


Figure 3 Glow of a processing plasma is seen through a port in the process chamber. The pink glow is due electrons exciting Argon atoms. (Source: TEL)

The electric sources used to create plasmas are varied: Direct current, Radio-frequency (from 100's of kHz to a few hundred MHz), or Microwave (mostly 2.45 GHz). The voltages are in the 100's of volts, and powers of several kWatt, up to 10's of kWatt can be used. Magnetic fields are sometimes used to enhance the plasma density or uniformity, or to enable operation at very low pressures. The choice of the plasma source depends on what is required of the plasma. Some sources operate better at very low pressures, while others at higher pressures.

The electric field heats the electrons in the plasma to temperatures between 10-40,000 Kelvin. A small fraction of them acquire enough energy to excite and ionize the background gas, forming a plasma. They also generate molecular and atomic species (known as radicals) that cannot exist under ordinary conditions. Because of the low pressure, the atoms, molecules, ions, and electrons suffer relatively few collisions on their way to the wafer. Otherwise, they would recombine, and we would lose all the benefits of having a plasma.

The choice of operating pressure is not arbitrary. While the pressure is low, the chamber is not at total vacuum. Instead, a carefully selected gas mix is flowing through the chamber. The different gases play different roles in the process. Some, like Argon, serve to ignite and support the plasma. Others, such as Oxygen or Fluorocarbon or metal-organic gases serve as sources of useful molecules, ions, or atoms that will perform etching of the wafers or deposit a 10's of nm thick layer of an insulating or conductive film. Finally, there are gases that are used as additives to fine-tune chemical reactions and to drive them towards a more favorable regime of operation.

The vacuum chambers where the processing occurs are designed to ensure a uniform flow of gas. The insides of the chamber are typically 20-30" in diameter, and up to 10" tall. The walls and all surfaces facing the plasma must prevent unwanted chemical reactions or the accumulation of particle-shedding material. They are also temperature controlled to manage chemical reactions on their surfaces.

The chamber dimensions, the gas pressure and electrical power sources define the properties of the processing plasma. The plasma is the medium for creation of the reactive species and their delivery to the wafer surface. Its properties (pressure, composition, dimension) determine the exact concentration and flow rate of the reactants to the wafer as well as the evacuation of the byproducts from the process chamber.

Wafer temperature management

The plasma presents a heat load to the wafer of about 700 W. This is about a half to a third of the maximum power consumption of a kitchen stove-top. Because of the very low gas pressure and the poor contact of the wafer to the stage that it is sitting on, this heat does not easily dissipate from the wafer to the stage that it is sitting on.

Without active cooling, the wafer would get red-hot. Such high temperature will damage or destroy the electronic components on the wafer. The wafer temperature is limited to about 400-500 °C.

To prevent temperature damage, the wafer is electrically "glued" to a cooled stage: a DC electric field is applied between the wafer and stage across a special insulator. This electric field makes the wafer "stick" to the stage (similar to when a balloon sticks to the wall). This process is called "electrostatic chucking".

This is still not enough. The points of contact between the wafer and the stage are too few to conduct heat. Also, at these low pressures, the microscopic gap between the wafer and the stage holds almost no gas molecules that would transfer heat from the wafer to the stage. To improve thermal contact between the chucked wafer and the stage a gas is released into the microscopic space. The gas used is typically Helium. It is used because of its very good thermal conductivity properties.

Etch directionality and RF bias

All ungrounded objects (i.e., electrically floating objects) in contact with a plasma develop a negative potential – this is a consequence of the large difference in the electron/ion temperature and electron/ion masses. This negative potential (also known as the plasma bias) accelerates ions towards the floating object, which in our case is the wafer.

The accelerated ions strike the wafer in a perpendicular direction. The energy of the impact is equivalent to about a temperature of 100,000 K. This effect is used to dislodge atoms from the wafer surface or to accelerate chemical reactions on the surface.

For many practical applications this impact energy is insufficient. An additional RF field is applied to the wafer stage to increase the impact energy. Impact energies used in microelectronic fabrication are equivalent to 1,000,000 K and higher. This is the technology of "RF biasing".

This technology is known as directional (or anisotropic) etching and is indispensable for the creation of vias or trenches with vertical walls (see Figure 4). Directional etching is one of two pillars of shrinking of microelectronic components, the other one being the projection of images of the transistors onto the wafers (lithography). In other words: lithography is used to form images of the patterns on the wafer. Directional etching is used to transfer these patterns into the underlying dielectric or metal layer.

This process of directional etching is used to define transistors, the interconnect metal lines and vias. It is also used to drill deep vias for 3D-NAND memory and capacitors for DRAM memory.

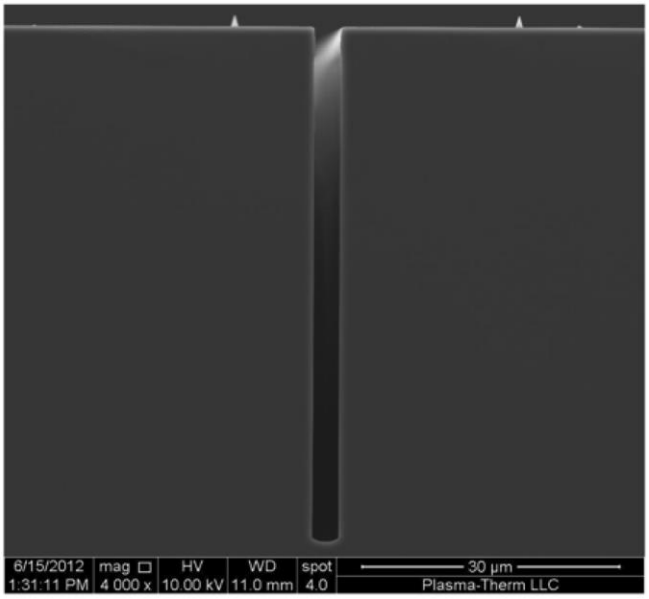


Figure 4: An example of a deep etch into Silicon using plasma technology (Huff, 2021). (Source: Micromachines)

Examples of plasma etching

Plasmas are used for several types of tasks in microelectronics fabrication: cleaning (removal/stripping of all surface material), etching (removal/stripping of desired material) and deposition.

The process of directional etching involves both chemical and physical processes. Plasma is used to generate the chemical species that will convert the solid layers into gaseous species. Other ions from the plasma serve the role to pre-activate the surface, making it available to interact with the chemical species. This effect, referred to as "synergy", increases the reaction rate by up to 10 times.

The first and simplest application that plasmas were used for is stripping of photoresist from the wafer. The photoresist is a carbon and hydrogen polymer (very similar to materials used in commercial products such as Plexiglas, Bakelite, tire rubber) that is used for transferring the circuit pattern from the template/mask onto the wafer using the process of lithography.

Oxygen plasmas were introduced to "burn-off" the photoresist. The burning-off is a chemical process: the oxygen plasma contains radicals: these are oxygen atoms, and they are very "greedy" to combine with the carbon and hydrogen on the film to form CO_2 and H_2O which are then evacuated. Sometimes, small amounts of even "greedier" species, such as Fluorine, are added to grab onto Hydrogen forming HF (Lieberman, 2005). This leaves exposed Carbon atoms, to which Oxygen can attach to form CO_2.

Removal of polymer film by conversion to volatile compounds (CO_2 and H_2O) is an example of using plasma to remove material by creating volatile species that are pumped out of the process chamber. The plasma is used to create atomic and molecular species that bind to the surface atom and to create these volatile species.

Silicon containing compounds (such as Si itself, SiO_2, and Si_3N_4) are similarly removed from the wafer by exposing them to fluorine or chlorine containing plasmas. For example, a chlorine containing gas (such as Cl_2) is used to etch Silicon. The plasma breaks the molecules liberating atoms of chlorine. They bind with Silicon atoms on the surface to create the volatile molecules such a $SiCl_2$ and $SiCl_4$ which are then evacuated from the chamber with the help of a vacuum pump (see Figure 5).

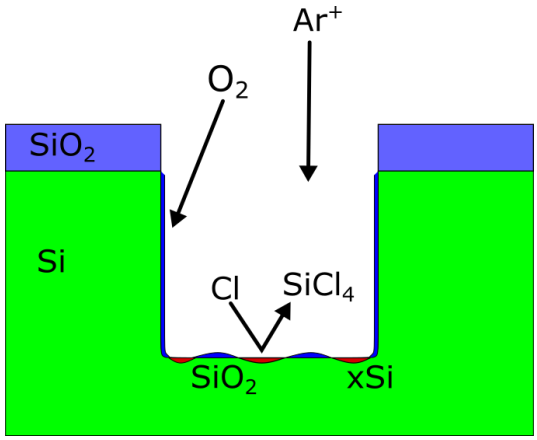


Figure 5: A schematic of plasma etching of Silicon. After the pattern in photoresist is transferred into SiO_2 (SiO_2) (not shown here, and also using plasma etching), Silicon (Si) is exposed to a $Ar/Cl_2/O_2$ plasma. Cl_2 attacks only Si and not SiO_2. As the line is etched, the exposed Si sidewalls are oxidized: Oxygen from the plasma binds to Si forming a thin layer of SiO_2. This "oxide" layer protects the sidewall from being etched by Cl_2. The bottom of the feature is also oxidized. But Argon ions (Ar+) vertically accelerated by RF biasing strike only the bottom of the feature (and not the sides) removing the thin oxide layer and exposing the underlying Si (xSi) to be etched away by Cl_2. The exposed Silicon (xSi) is etched by Chlorine atoms, liberating the gaseous $SiCl_4$. (Source: TEL)

Practical considerations

While it is relatively easy to engineer a plasma that will perform a particular task on a small sample such as a 1cm×1cm coupon, it is much harder to ensure that this process performs equally well across the whole wafer. Plasmas tend to be non-uniform because of the plasma losses at the chamber walls. On the other hand, the process across a 300mm wafer has to be very uniform. In modern applications, the thickness variation across a wafer must be as little as 30 atoms.

The natural property of the plasma non-uniformity is counteracted by careful engineering and optimization of the process chamber. This involves optimization of the chamber shape, the radial intensity profile of the electric fields that generate the plasma, and the flow of gasses in and out of the chamber. For processes that are temperature dependent, the temperature

across the wafer, and the temperature of all chamber components is carefully controlled by zonal heating or cooling.

The selection of chemical species that are used for plasma processing is very involved. Not only the reactions on the wafer surface matter. If the gases or by-products react with the chamber walls, the process uniformity will be degraded.

Carbon-containing molecules tend to stick together, creating particles (or dust) in the plasma. When these particles fall onto the wafer, the resulting circuits are defective, reducing yield.

Future

Leading edge microelectronics have reached the stage where further reduction in feature size is deemed impractical. Instead, the industry is "going vertical": transistors stacked at top of each other, and chips stacked on top of each other (Figure 6). The manufacturing technology enabling 3D microelectronics is under active development (IRDS More Moore, 2022) with plasma continuing to play a key enabling role.

New types of computing circuits, better suited for machine learning and AI are under development. These are known as neuromorphic circuits. They operate with lower precision than traditional CPU's (central processing unit), but also consume much less power, while being much faster at performing some types of arithmetic operations. They use novel devices and materials.

Technology advances like these will continue to drive the further evolution of plasma etching equipment and process. The work of designing and manufacturing the future plasma tools will involve many mechanical, chemical, electrical, and computer control engineers. The teams that develop recipes for wafer processing consists of technicians, engineers, and PhD's skilled in many different fields: physics, chemistry, material science, and system control.

Source: TEL estimates

Year of HVM (20k/month)	2022~23	2024~2025	2027~28	2029	2031	2033	2035
Node	3nm	2nm	14A	10A	7A	5A	3A
Device	2~1 Fin	GAA NS	Forksheet	CFET	2nd Gen. CFET	3rd Gen. CFET	IL/HK IL/HK 2D material: TMDC MoS_2, WS_2, $MoSe_2$, WSe_2 etc.

Figure 6: Transistor roadmap. The 3nm node will be the last one using fin-FET based devices. It cannot be shrunk further. All future notes, starting with the 2nm node, will use nano-sheets for channels. Starting with node 10A, the N and P transistors will be stacked on top of each other. (Source: TEL)

Further reading

Early History of plasma etching is described by in section II of (Donnelly, 2013). Two readable descriptions of plasma etching in semiconductor industry are (Lee, 2014) and (Kanarik, 2020). The roadmap for microelectronics is published by the IEEE. For an overview, see (IRDS Executive Summary, 2022).

Bibliography

Huff, M. (2021). Recent Advances in Reactive Ion Etching and Applications of High-Aspect-Ratio Microfabrication. *Micromachines*, 991.

IRDS Executive Summary. (2022). *International Roadmap for Devices and Systems, 2022 Update: More Moore.* IEEE.

IRDS More Moore. (2022). *International Roadmap for Devices and Systems, 2022 Edition, Executive Summary.* IEEE.

Kanarik, K. J. (2020). Inside the mysterious world of plasma: A process engineer's perspective. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 38*(3), 031004

Donnelly, V. M. et al. (2013). Plasma etching: Yesterday, today, and tomorrow. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 31*(5), 050825.

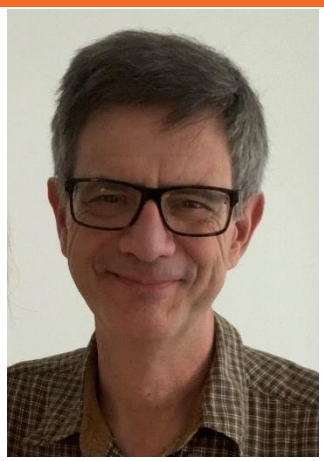
Lee, C. G. et al. (2014). The grand challenges of plasma etching: a manufacturing perspective. *Journal of Physics D: Applied Physics, 47*(27), 273001.

Lieberman, M. A. et al. (2005). *Principles of Plasma Discharges and materials Processing.* Wiley Interscience.

Text and images by M. Vukovic
Edited by M. Laroussi

The Plasma Connection is a publication of the IEEE Nuclear and Plasma Sciences Society.

THE PLASMA CONNECTION



ABOUT THE AUTHOR

Mirko Vukovic's journey into plasma physics started at the Boris Kidrič Institute in Vinča, Yugoslavia, in 1983. As a young researcher, he worked there on the magnet design for a plasma source for highly charged ions driven by an Electron Cyclotron Resonance source.

In 1995 Mirko received a Ph.D. from the University of Wisconsin - Madison. His research topic was Alfven Wave current drive in a tokomak plasma. Since graduation he has worked in the field of low-temperature plasma in semiconductor equipment manufacturing industry, mainly at Varian Research in Palo Alto, California, and then with Tokyo Electron in Gilbert, Arizona, and Albany, New York.

He has worked on RF equipment design and characterization, RF diagnostics, plasma probes and plasma modeling. Mirko also wears many other hats in semiconductor equipment engineering: maintenance of EDA software systems and Linux computers, low pressure gas flow modeling, fluid and thermal analysis. He is author or co-author of 20 US patents.

Mirko is also active in the US low temperature plasma physics community. As local secretary of the Gaseous Electronics Conference (GEC), he organized its 2009 Conference in Saratoga Springs, NY. He was also GEC chair for the 2015 and 2016 conferences in Honolulu, HA, and Bochum, Germany respectively.